

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A high power semiconductor device for a radio communication system, comprising:

a compound semiconductor substrate having a resistivity less than 1.0×10^8 Ohm-cm at least at a surface thereof;

a buffer layer formed on the compound semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having a high power active element for radio communication formed therein, wherein said substrate, buffer layer and active layer, together form said high power semiconductor device.

Claim 2 (previously presented): The semiconductor device as claimed in claim 1, wherein the compound semiconductor substrate has a resistivity less than 0.6×10^8 Ohm-cm.

Claim 3 (previously presented): The semiconductor device as claimed in claim 1, wherein the active layer is formed at a position within $5.0 \mu\text{m}$ from the surface of the compound semiconductor substrate.

Claim 4 (previously presented): The semiconductor device as claimed in claim 1, further comprising an electrode layer formed on another surface of the compound semiconductor substrate.

Claim 5 (previously presented): The semiconductor device as claimed in claim 4, wherein the electrode layer is not electrically connected to any power supply potential of the semiconductor device.

Claim 6 (previously presented): The semiconductor device as claimed in claim 4, wherein the electrode layer is connected to one power supply potential of the semiconductor device.

Claim 7 (previously presented): The semiconductor device as claimed in claim 1, further comprising:

a source electrode and a drain electrode formed on the active layer, separated from each other so as to establish a channel region, and
a gate electrode formed above the channel region.

Claim 8 (previously presented): The semiconductor device as claimed in claim 7, wherein the active layer has 2-Dimensional Electron Gasses.

Claim 9 (cancelled)

Claim 10 (currently amended): A high power semiconductor device for a radio communication system, comprising:

a compound semiconductor substrate having a resistivity less than 1.0×10^8 Ohm-cm at least at a surface thereof;

a buffer layer formed on the compound semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having a high power active element formed therein,

wherein the compound semiconductor substrate has a resistivity of more than 1.0×10^8 Ohm-cm in total, and wherein said substrate, buffer layer and active layer, together form said high power semiconductor device.

Claim 11 (canceled).

Claim 12 (previously presented): The semiconductor device as claimed in claim 1, wherein the buffer layer has a GaAs/AlGaAs super lattice structure.

Claim 13 (previously presented): The semiconductor device as claimed in claim 1, wherein the GaAs/AlGaAs super lattice structure includes undoped GaAs layers having a carrier concentration less than $1 \times 10^5 \text{ cm}^{-3}$.

Claim 14 (currently amended): The semiconductor device as claimed in claim 12, wherein the GaAs/AlGaAs super lattice structure includes ~~undoped~~ undoped AlGaAs layers have a carrier concentration less than $1 \times 10^{16} \text{ cm}^{-3}$.

Claim 15 (previously presented): The semiconductor device as claimed in claim 1, wherein the active layer is doped with Is to a concentration of $1 \times 10^{17} \text{ cm}^{-3}$.

Claim 16 (previously presented): The semiconductor device as claimed in claim 1, wherein the compound semiconductor device substrate is a GaAs substrate.

Claim 17 (currently amended): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is ~~disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer~~

~~inhibits~~ configured sufficient to inhibit electrical field concentration in the active layer upon activation of the semiconductor device.

Claim 18 (currently amended): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is ~~disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer~~ inhibits configured sufficient to inhibit accumulation, at the interface between the low-resistance substrate layer and the buffer layer, of electrons leaking from the active layer from accumulating at the interface between the low-resistance substrate and the buffer layer.

Claim 19 (currently amended): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is ~~disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer~~ inhibits configured sufficient to inhibit domain generation in the buffer layer under high power operating conditions, upon activation of the semiconductor device.

Claim 20 (previously presented): The semiconductor device as claimed in claim 10, wherein the buffer layer has a GaAs/AlGaAs super lattice structure.

Claim 21 (previously presented): The semiconductor device as claimed in claim 20, wherein the GaAs/AlGaAs super lattice structure includes undoped GaAs layers having a carrier concentration less than $1 \times 10^{15} \text{ cm}^{-3}$.

Claim 22 (previously presented): The semiconductor device as claims in claim 20, wherein the GaAs/AlGaAs super lattice structure includes undoped AlGaAs layers having a carrier concentration less than $1 \times 10^{16} \text{ cm}^{-3}$.

Claim 23 (previously presented): The semiconductor device as claimed in claim 10, wherein the active layer is doped with Is to a concentration of $1 \times 10^{17} \text{ cm}^{-3}$.

Claim 24 (previously presented): The semiconductor device as claimed in claim 10, wherein the compound semiconductor device substrate is a GaAs substrate.

Claim 25 (currently amended): The semiconductor device as claimed in claim 10, wherein the super lattice buffer layer is ~~disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer~~ inhibits configured sufficient to inhibit electrical field concentration in the active layer upon activation of the semiconductor device.

Claim 26 (currently amended): The semiconductor device as claimed in claim 10, wherein the super lattice buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer inhibits configured sufficient to inhibit accumulation, at the interface between the low-resistance substrate layer and the buffer layer, of electrons leaking from the active layer from accumulating at the interface between the low-resistance substrate and the buffer layer.

Claim 27 (currently amended): The semiconductor device as claimed in claim 10, wherein the super buffer layer is disposed between the compound semiconductor substrate and the active layer such that, when the semiconductor device is activated, the super lattice buffer layer inhibits configured sufficient to inhibit domain generation in the buffer layer under high power operating conditions, upon activation of the semiconductor device.

Claim 28 (new): The semiconductor device as claimed in claim 10, wherein said compound semiconductor substrate comprises:

a support substrate layer having a resistivity of more than 1.0×10^8 Ohm-cm, and
a substrate surface layer provided on said support substrate layer having a resistivity of less than 1.0×10^8 Ohm-cm.